

Magtrak Board

A specific hardware for Vision Applications

Technical Reference

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Preface

Chapter 1 - Introduction

An overview of this device and its features, in which will be found the jumper configuration and the pin in and out connectors.

Chapter 2 - Host requirements and operation

Specifies the host requirements to support the Magtrak board.

Chapter 3 - Device schematics

Contains the schematics for the Magtrak.

Introduction

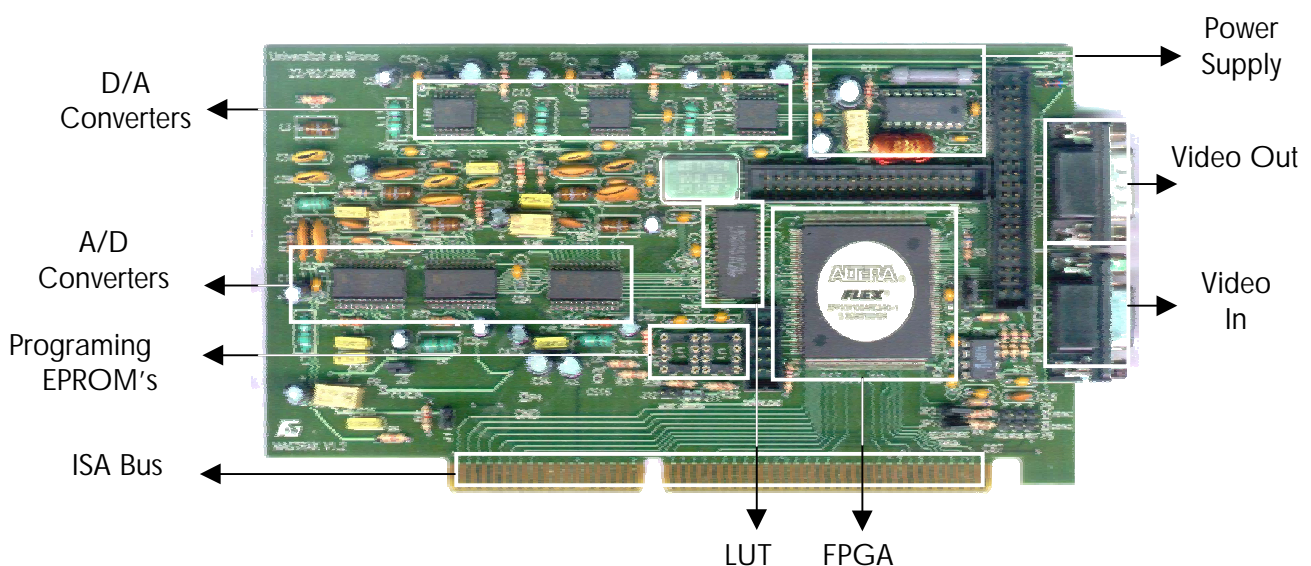
Computer vision is a technology used in a great number of industrial applications.

One of the problems frequently encountered in industry is knowing the position of a certain group of objects in a given environment. This can be solved by using an Image Process Board and a specific software which perform the necessary computing tasks. This solution is very flexible but in some cases isn't quick enough.

Another solution, as we propose here, is a specific hardware able to perform the computing tasks very quickly and efficiently.

The Magtrak Board is able to determine the position of 15 objects ,for example, at 50 frames per second. (20 ms)

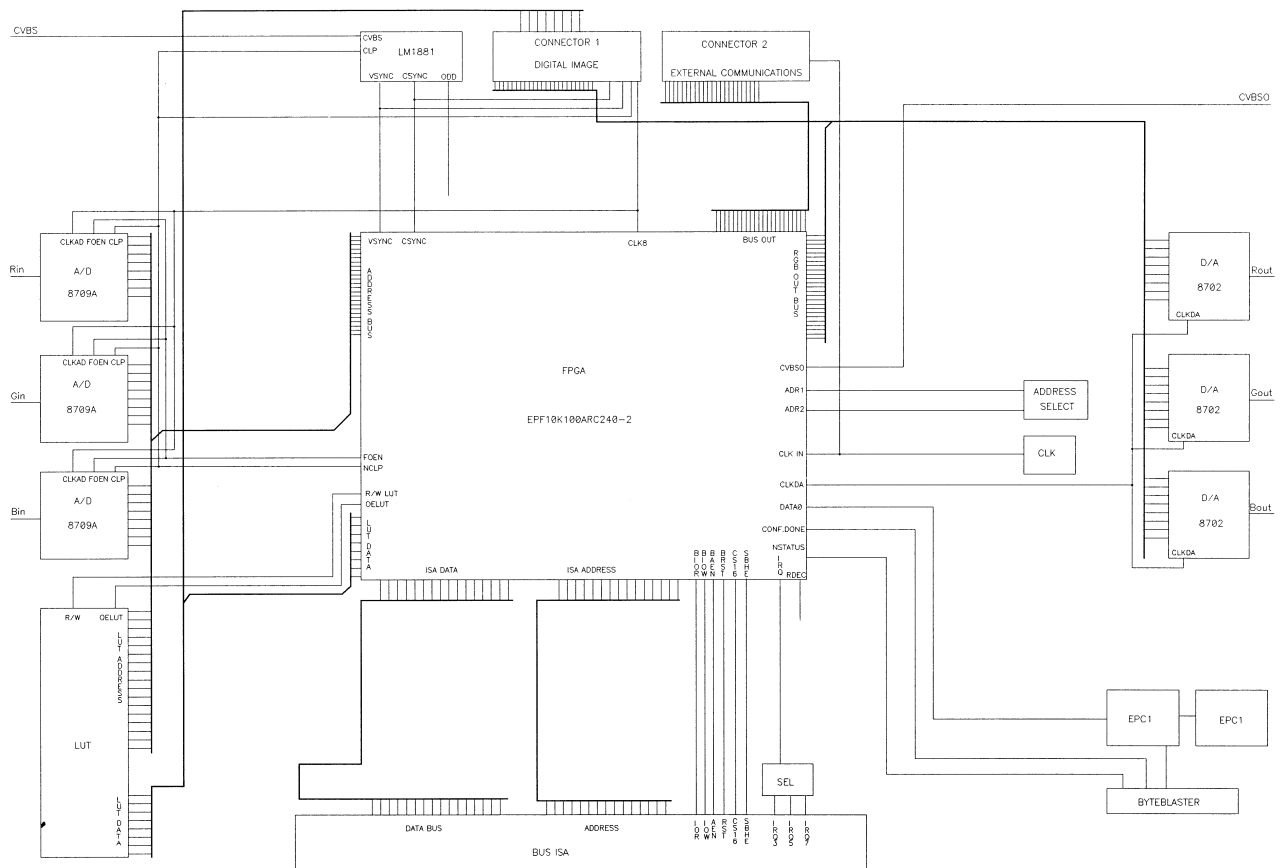
The figure below shows the Magtrak board.



The Magtrak is a PC board connected to an ISA bus (16 bits communication).

The heart of this board is a FPGA (EPF10K100ARC240-2, Altera). Also, there are A/D and D/A converters of 8 bits precision.

The figure below shows the block diagram of this device.



Key features

- Video in (RGB+SYNC PAL system)
- A/D converters
- Programmed EPROM's
- FPGA device (main part of the board)
- LUT memory
- Bus ISA connector
- D/A converters
- Video out (RGB+SYNC PAL system)

Jumpers configuration

Jumper	Description	Value
J1	Reserved (always insert)	Insert
J2	Video input selection	<div><div>Cvbs in</div><div>G in</div></div>
J3	Reserved (always insert)	Insert
J4	Video output selection (B)	Normal <div></div> Inverted <div></div>
J5	Video output selection (G)	Normal <div></div> Inverted <div></div>
J10	Video output selection (R)	Normal <div></div> Inverted <div></div>
J11	FPGA download mode	SRAM <div></div> EPROM <div></div>
J12	FPGA download mode	SRAM <div></div> EPROM <div></div>
JP2	See next section	

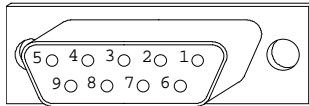
On
 Off

Table 1

Interruptions

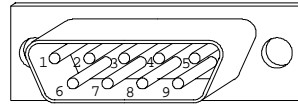
The Magtrak board can generate hard interruptions to deliver new data for processing to the PC. The user can choose from among the IRQ3, IRQ5 or IRQ7 by jumpers.

Connectors



Input plug

Pin 1	Input R
Pin 2	Input G
Pin 3	Input B
Pin 4	Input SYNC
Pin 5	NC
Pin 6	GND R
Pin 7	GND G
Pin 8	GND B
Pin 9	GND SYNC



Output plug

Pin 1	NC
Pin 2	GND
Pin 3	Output R
Pin 4	Output G
Pin 5	Output B
Pin 6	+12V
Pin 7	NC
Pin 8	CVBSO
Pin 9	NC

Host Requirements and operation

The following are the minimum host system requirements for the Magtrak board:

- IBM PC/AT compatible computer
- One 16-bit slot
- 8 megahertz I/O bus clock speed
- 8 bytes of I/O space
- 5 volts , 1.5 ampere.

It is possible install to up to four Magtrak boards in the same PC. The address for access is configurable by two jumpers placed in the same boards. Then you will need four ISA slots in your PC.

JUMPER2	JUMPER1	BASE ADDRESS
0	0	300h
1	0	340h
0	1	380h
1	1	3D0h

Table 2

Before connecting the board....

You have to turn the potentiometer (R22) to the right, (about 10 turns). Then the supply voltage must be adjusted to 3.3 volts with a tester and fine turning of the potentiometer.

Adjusting the board....

You have to turn the color adjust potentiometers to the left (about 10 turns). Tuning is more precise with the program (adjust.exe) as we will explained in the following.

- 1) Connect a color image bar to the input and execute the program.
- 2) Connect a monitor with which can watch the image and a cursor to the output.
- 3) Place the cursor on the white bar and make note of the values of the R, G and B components.
- 4) By adjusting the potentiometers, you have to obtain the value 255 for each component.

The best adjustment is achieved when the value is between 254 and 255.

Address range used by Magtrak

This board uses several addresses to communicate with the PC and execute the functions implemented inside. Depending on the project implemented in the FPGA this address range can change.

Reprogramming the FPGA

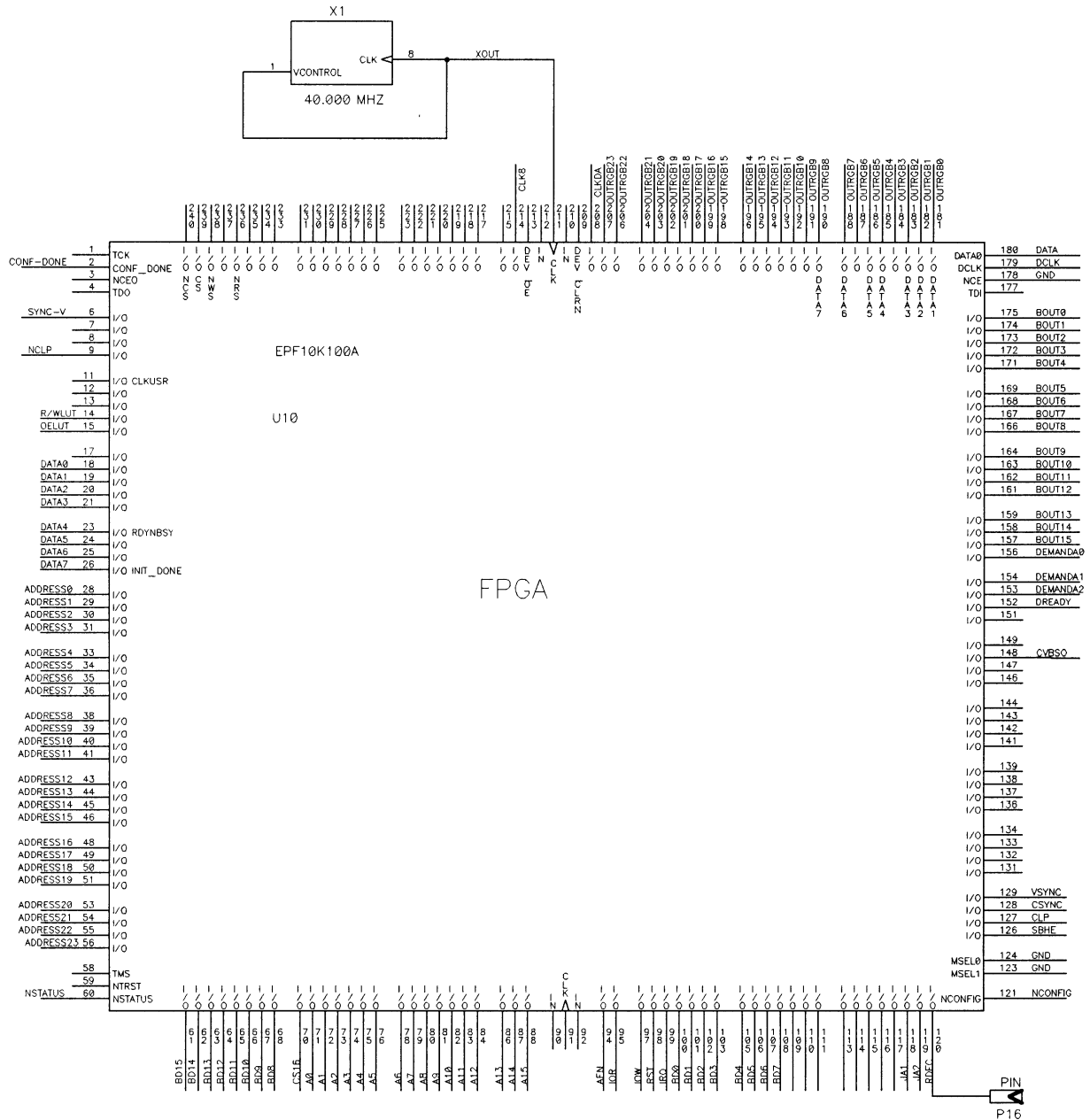
The Magtrak board could be reprogrammed by correctly setting jumpers J11 and J12, as we show in table 1.

It's possible to choose two modes:

1. Using the SRAM or byteblaster connector, and downloading the project with the MAX PLUS II software.
2. Using two serial ROMS placed on the board, near the FPGA. These kinds of memories can't be reprogrammed therefore if you wish to modify the project you have to change the serial ROM memories.

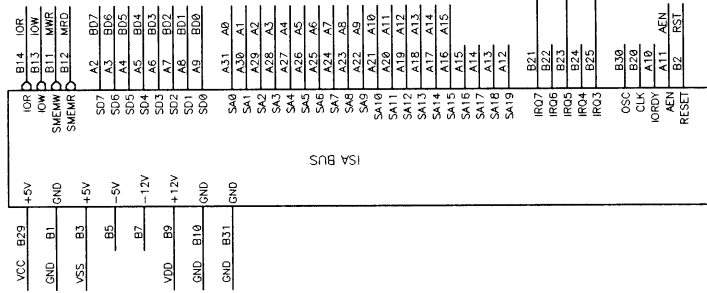
Device Schematics

This chapter contains the schematics for the Magtrak board.



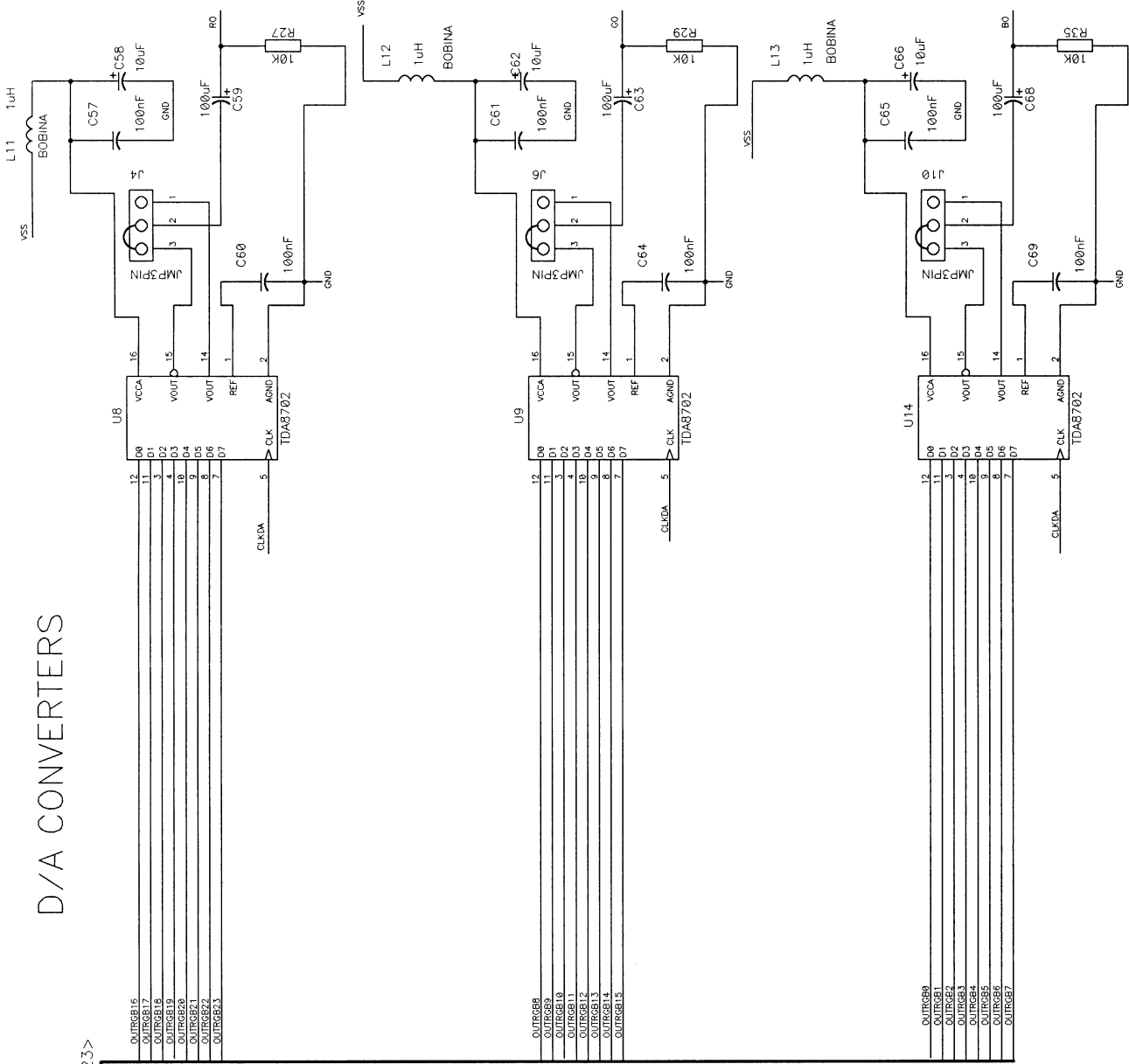
ISA BUS

VAL
CONNECTISA16
C67

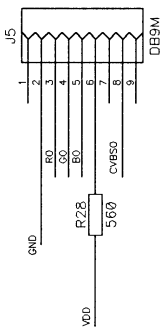


D/A CONVERTERS

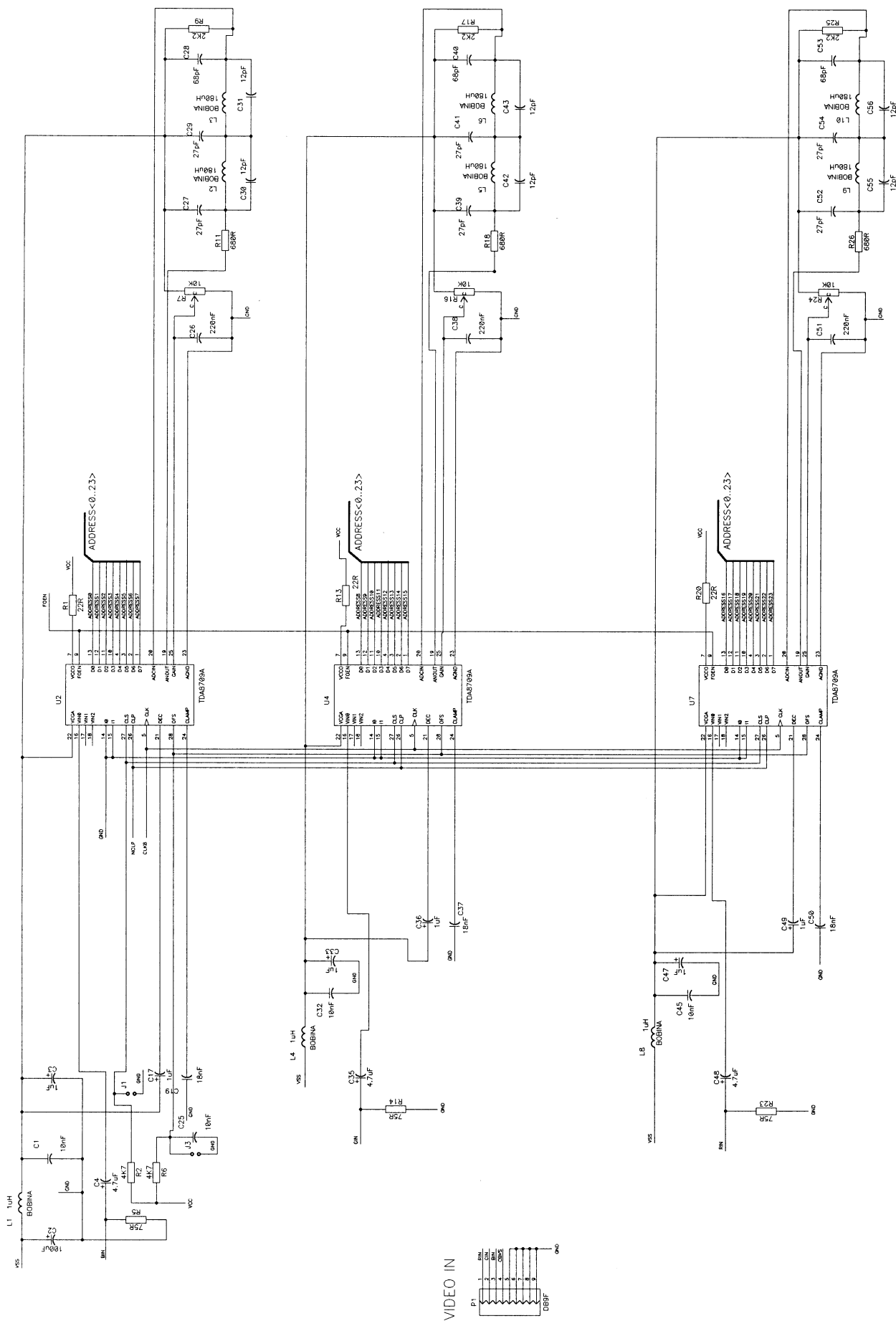
OUTRGB<0..23>



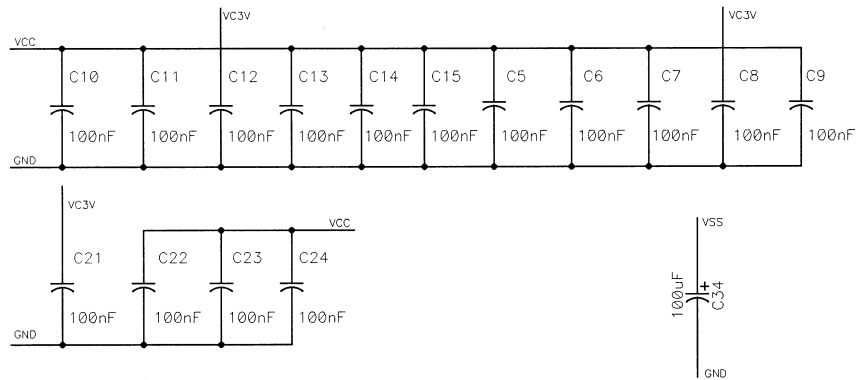
VIDEO OUTPUT



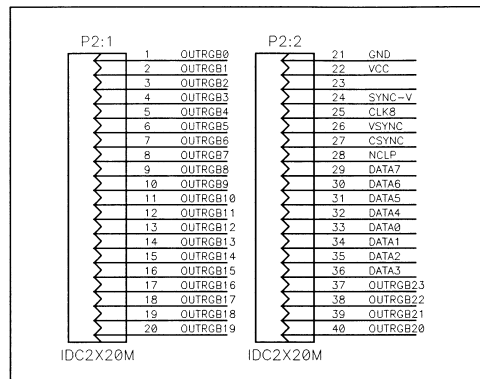
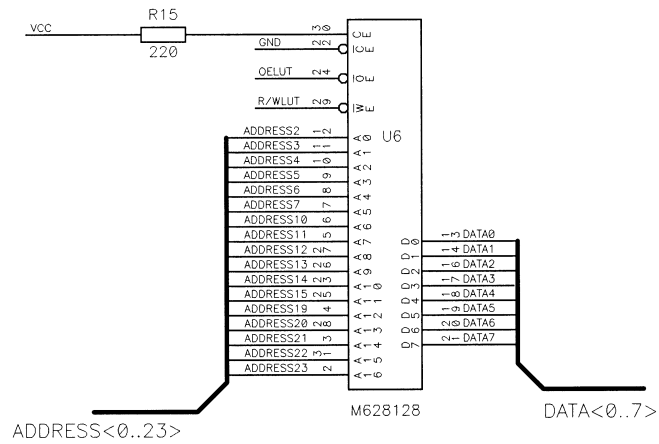
A/D CONVERTERS



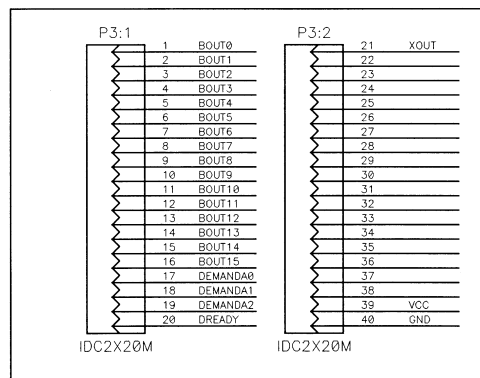
DECOUPLING CAPACITANCES



LUT



VIDEO DIGITAL CONNECTOR



EXTERNAL COMMUNICATIONS

