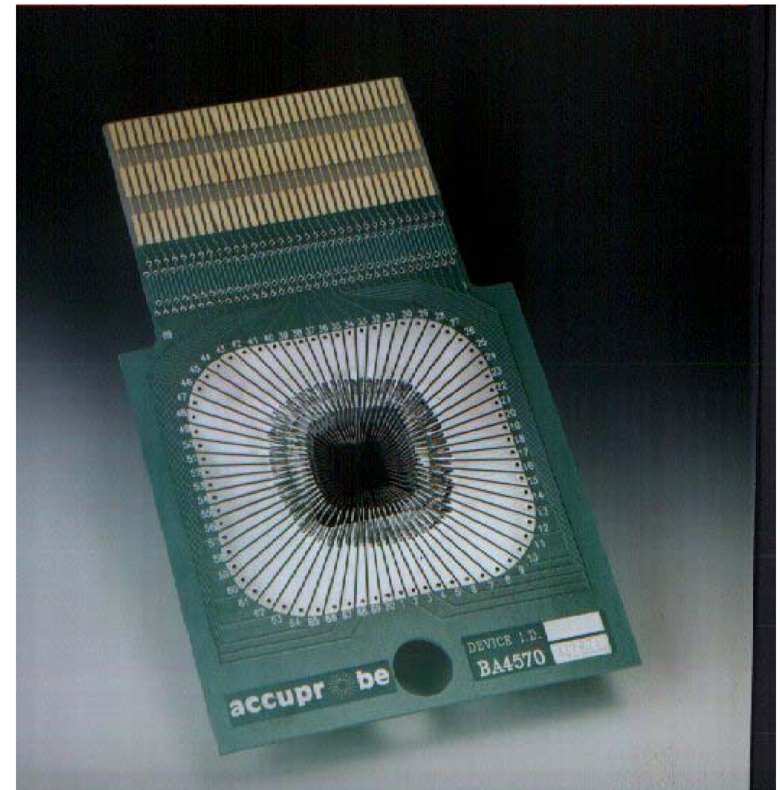
Additional Slides for Lecture 16

Test Hardware

- Your chip is designed to be assembled in a package
- The package is designed to be attached to a PC board
- Stimulus is applied to the pins of the chip by other chips or by peripheral devices
- Need to emulate this as part of the test environment
  - Emulate the package during wafer test
  - Emulate the system after the chip is assembled

Emulating the package: probe cards

- Chip packages can be expensive
  – Fifty cents to hundreds of dollars
- Want to test chips before they are assembled
  – Saves package cost for bad dies
- Use probe card to probe chips at the wafer level
  – Fine probe tips make contact with all the pads at once



Source - Accuprobe

Emulating the System: Automated Test Equipment

- Wafer probe is generally just an initial screen
- Still need to test final packaged parts
  - Testing them *in situ* usually isn't practical
- Generally done on Automated Test Equipment (ATE)
  - Can drive (semi-) arbitrary test patterns on device pins
  - Can observe the data that the chip sends back

Automated Test Equipement

- Fairly expensive machines
  - $1M and up
- Cost is proportional to number of channels
  - A channel drives or observes a single pin on the device
  - Channel counts generally range from 32 up to 1024
  - Possible to test multiple devices in parallel

Agilent 95000

Handlers

- In a production test environment to get parts on and off the tester quickly
- Handler interfaces to tester and shuffles chips off/on it
  - Can handle thousands of devices per hour

Source: Advantest

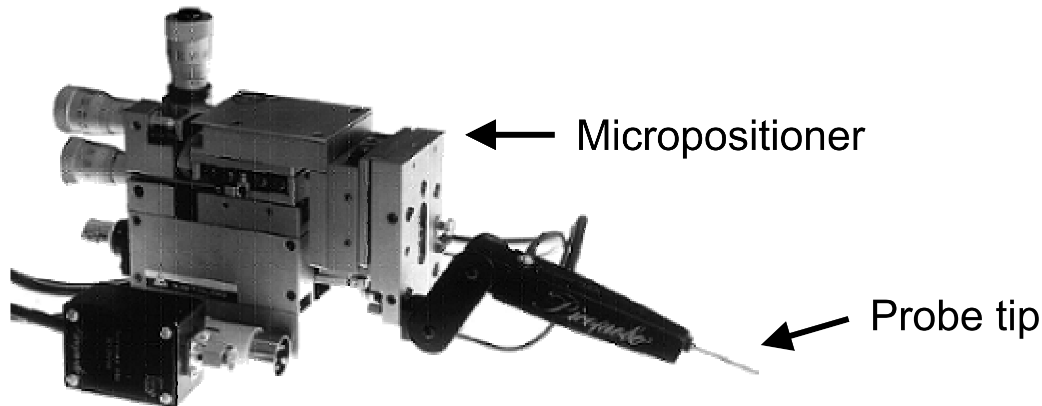
Temperature testing

- Chips are slower at high temperature
- Transistor thresholds are higher at low temperature
- Need to test at different temperatures to ensure functionality
- Thermal equipment can set die temperature
- Thermal streamers
  - Fast, wide temperature range
  - Not popular with humans
- Peltier devices
  - Slower
  - Good for debug

Source: Temptronic

Picoprobing

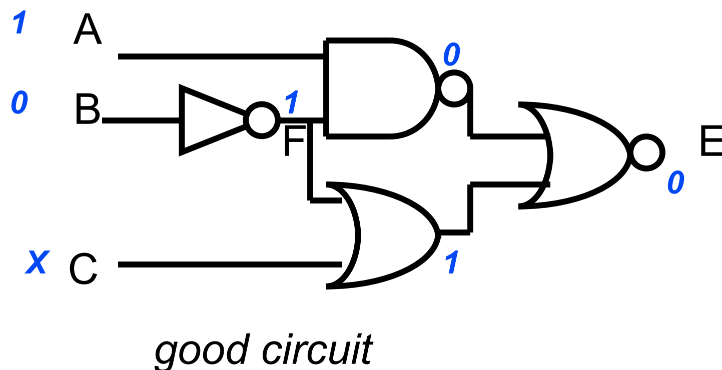
- Touch down on surface of die with extremely fine whisker
  - Tip can be as small as 0.1μ
  - Moderate loading on internal nodes: 100fF, 10MΩ
- Top of die typically covered with Silicon Nitride for protection
  - Need to open hole to allow probing



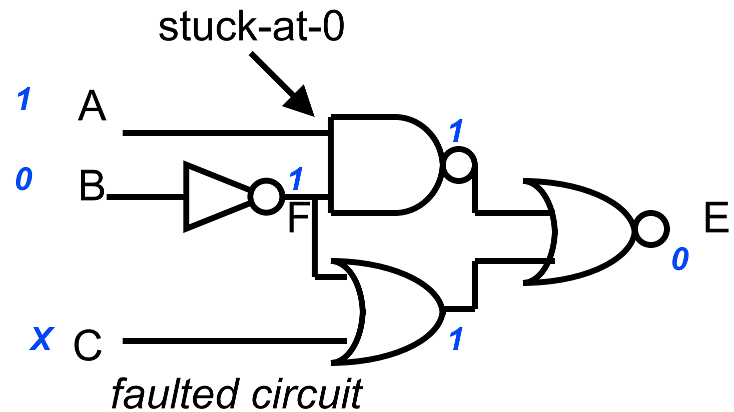
source: GGB industries

Reconvergent Fanout

- Controllability and Observability much more complicated with reconvergent fanout
- Can't independently set the inputs
- No value of B will make a stuck-at-0 both observable and controllable



good circuit



faulted circuit

Looking Outward: Board test

- Also need to test Printed Circuit Boards (PCB's)
  - Catch soldering errors, etc.
- Traditional Style: Bed of Nails Tester
  - Contacts to vias on board
- Less useful with surface mount components
  - Harder to get access

Adding and Using JTAG

- The JTAG standard defines a Test Access Port (TAP)
  - Five pins: Reset, Data In, DataOut, Clock, Test Mode Select
- JTAG ports for multiple devices can be connected in chain
  - Single test port for entire printed circuit board
- JTAG is pretty much a requirement for large boards
  - Impossible for system vendor to test/rework otherwise
- Most ASIC flows can automatically insert it

Next Generation JTAG (1149.6)

- Current JTAG spec only works for level sensitive circuits
- Many high speed links are now AC coupled and differential
  - They don’t pass DC signals
  - JTAG 1149.1 won’t work with them
- New specification being devised to test AC coupled I/O’s
  - JTAG 1149.6
  - Pulses data on lines to get through coupling caps