Lecture 2

Fabrication and Layout

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Overview

- Reading
  - W&E 3.1(scan), 3.2.1, 3.3.1 - Fabrication
  - W&E 3.4-3.4.3 - Design Rules

    (λ rules are really not that bad)
- Introduction

  The whole IC business is based on the fact that complex circuits can be 'printed' on a silicon wafer, thus the cost of the chip depends mainly on its size and not the number of devices (the complexity of the picture). This fabrication process is possible because of special properties of semiconductors and in particular the semiconductor silicon. This lecture will briefly review some semiconductor properties, and then describe how chips are made. The fabrication discussion will motivate the design rules that need to be followed for layout.

What Do We Need to Build?

Transistors

- Need nMOS and pMOS
- How are these built?

Wires

- Many levels of real metal wires (mostly aluminum or copper)
  - We we see that we need low resistance (high conductivity)
- Oxide insulator between metal layers
- Contacts (hole in the oxide) between adjacent layers
  - Adjacent layers only
  - To connect M1 to M3, need to connect M1 to M2, and M2 to M3

- Let's digress and look at how to build a transistor
  - Physics, and materials

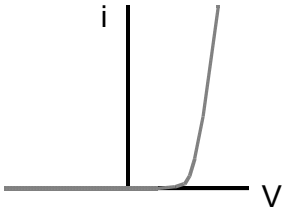
+ Silicon

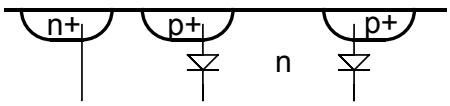
IC fabrication depends on two properties of silicon:

- It is a semiconductor
  - Conductivity can be changed by adding impurities
  - These impurities, called dopants, can create either n-type or p-type regions.
- Its oxide is very stable
  - It is SiO_2 , which is quartz or glass (amorphous)
    - 'silicon rust' is glass
  - Great for sealing stuff from impurities
  - Can be selectively patterned.
  - Etching can remove SiO_2 without harming Si.
  - Stable grown oxide is the great advantage of Si over Ge or GaAs.

+ Doping

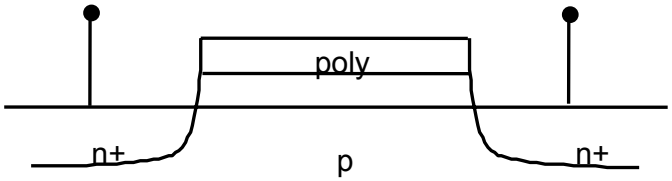
- Adding arsenic or phosphorous to the intrinsic silicon increases its conductivity by adding ‘free’ electrons. Silicon with electron carriers is called n-type silicon, since the current is carried by particles with negative charge.
- Adding boron to intrinsic silicon increases its conductivity by adding ‘free’ holes. Holes are like electrons, but have a positive charge, so this type of material is called p-type silicon.
- The junction between n-type and p-type regions have special properties – it forms a diode.





Note that the doping also adds fixed charge in addition to the mobile charge so the region remains neutral. n doping adds fixed positive charge and mobile electrons, and p doping is fixed negative charge and mobile holes

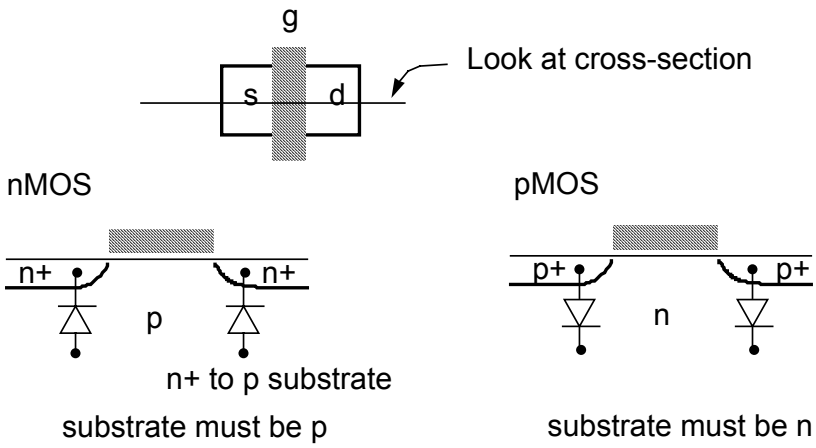
+How to Build a Transistor



Diffusion is made by adding (diffusing) impurities into the silicon

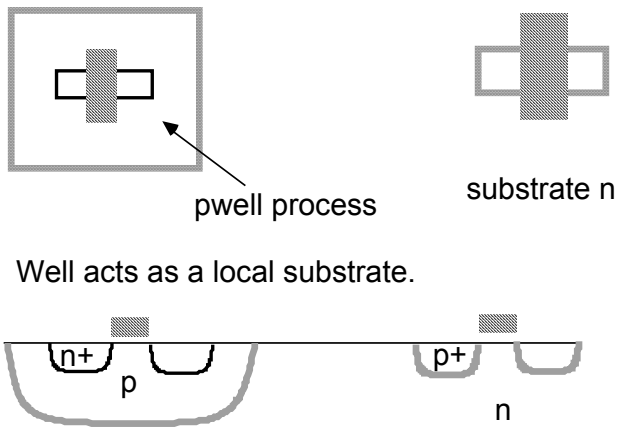
- n+(p+) diffusion means the region has a lot of impurities (dopants) which improves it conductivity (and hence lowers its resistance)
- p (n) regions are more lightly doped
- p region is formed first, and then the n+ over dope parts of the p region to form the n+ regions
- n+ dopant is added after the poly is down so poly blocks dopant

CMOS Has Two Transistor Types



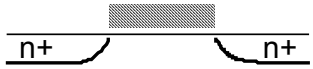
- CMOS devices require two types of substrate for isolation of transistors
- n-type for pMOS
- p-type for nMOS

Wells: Local Substrates

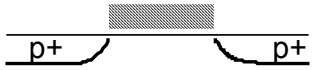


- Fabricators can choose to make the base wafer n-type (add pwells) or p-type (add nwells), or choose to add both, ("twin" wells).

Well Requirement



p ← tied to most negative potential Gnd.



n ← tied to most positive potential V_{dd}

- Well must to be tied to a power supply to keep the isolation diodes reversed biased. This is accomplished by using well contacts (ohmic connection to the well)

- Well Contacts

- Formed by placing p+ doped region in a pwell
  or n+ doped region in a nwell
- These regions make good electrical contact (ohmic, not diode) to the well and thus the well potential is made equal to the potential of the diffusion
- Need to have at least one well (substrate) contact in each well.
- These contacts are then connect to the correct power supply to ensure that the diodes are always reversed biased.

What is On a Chip

Transistors

- Requires silicon substrate, wells
- Diffusion (two types), poly

Wires

- Many levels of real metal wires (mostly aluminum)
- Oxide insulator between metal layers
- Contacts (hole in the oxide) between adjacent layers

Now that we have a quick overview of what we are building, lets delve in more detail into how to build it.

Fabrication

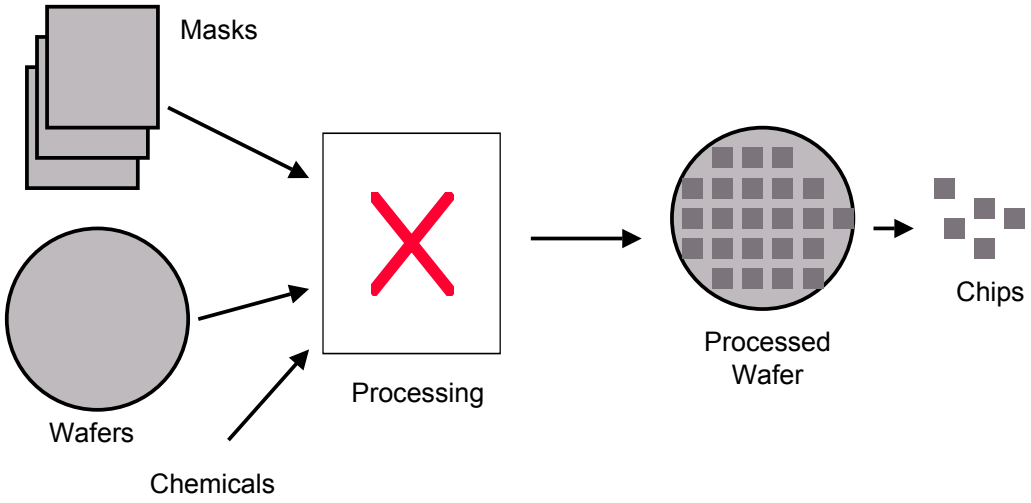
The process used that creates these devices/wires.

- Look at how to create:
  - Working transistors
    - ndiff, pdiff, wells, poly, transistors, threshold adjust implants
  - Wires
    - contacts, metal1, via, metal2

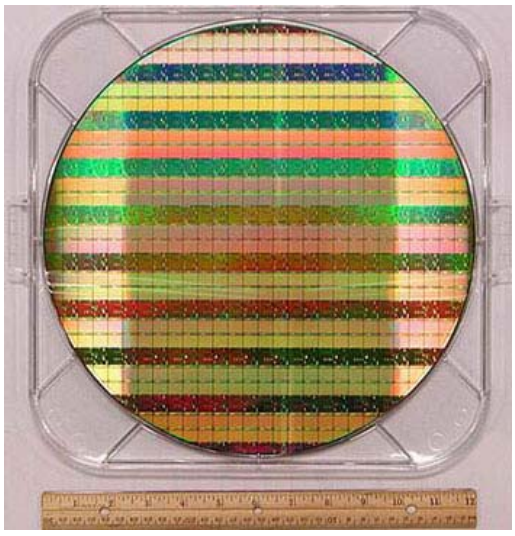
Fabrication is pretty complex.

- There are whole classes at Stanford devoted to it.
- Give a brief overview of the process, for background.
- Want to understand origin of layout rules / process parameters
  - The abstractions of the process for the designer (us).

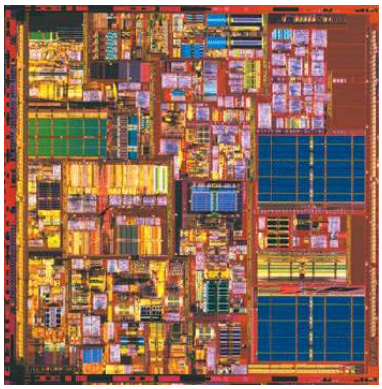
Making Chips



Making Chips



Intel 300mm wafer



Pentium 4 die size:

11.45mm x 11.45 mm

0.13 μm

+ Basic Fabrication Step

Two parts:

- Transfer an image of the design to the wafer
- Using that image as a guide, create the desired layer on silicon
  - diffusion (add impurities to the silicon)
  - oxide (create an insulating layer)
  - metal (create a wire layer)

Use the same basic mechanism (photolithography) to do step 1.

Use three different methods to do step 2.

- Ion Implant - used for diffusion. Shoot impurities at the silicon.
- Deposition - used for oxide/metal. Usually from chemical vapor (CVD)
- Grow - used for some oxides. Place silicon in oxidizing ambient.

Basic Processing

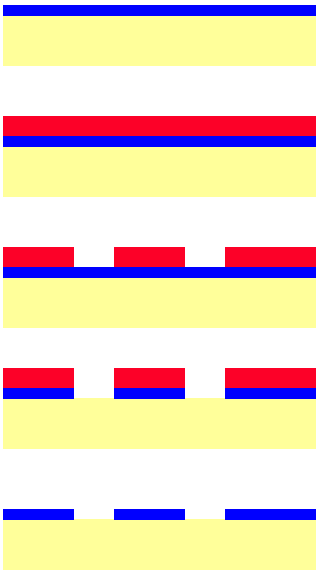
Start with wafer at current step

Spin on a photoresist

Pattern photoresist with mask

Step specific processing
etch, implant, etc...

Wash off resist

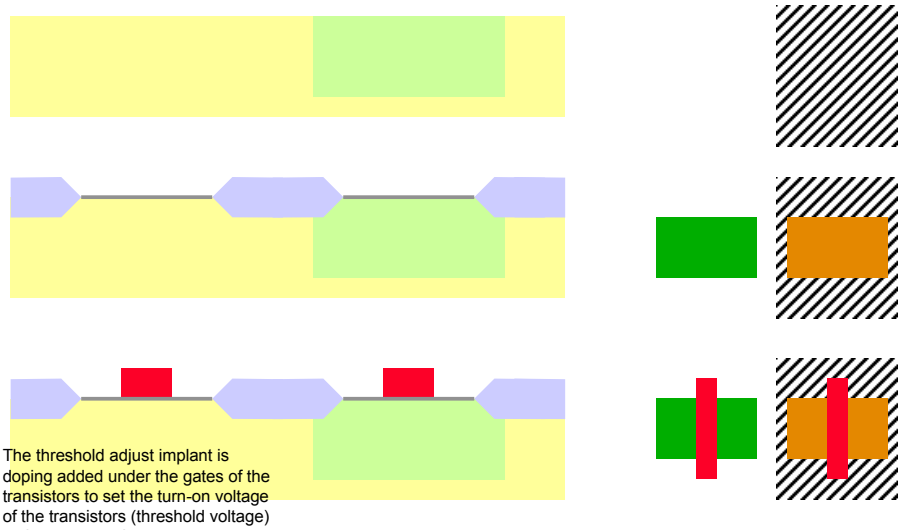


+ Photolithography

- To transfer the pattern onto the wafer, one first needs to have an image to project. While this can be done using some scanning technology directly from the design database to the wafer (like generating a TV picture), it is usually done using a two step process:
  - First a glass plate with a image of the pattern etched in chrome is generated from the design database. This glass plate is called a mask, and serves the same function of a negative in photography.
  - This image is optically projected onto wafer using a “projection-aligner” which is very much like an enlarger in photography. It projects the image of the mask onto the silicon wafer. Resolution is impressive.
- This two step process is used since scanning data serially is an expensive step since it takes a long time on an expensive machine. By generating a mask which can print on a large number of wafers, the cost per wafer can be made small. (But implies that you want lots of parts).

Making Transistors

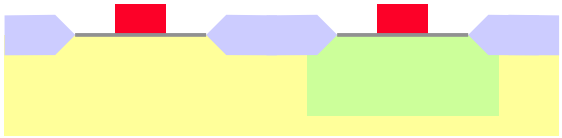
1. Implant N-Well
2. Define thin oxide grow field oxide, implant doping to adjust transistor threshold
3. Deposit and etch polysilicon

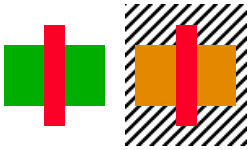


The threshold adjust implant is doping added under the gates of the transistors to set the turn-on voltage of the transistors (threshold voltage) to the correct value.

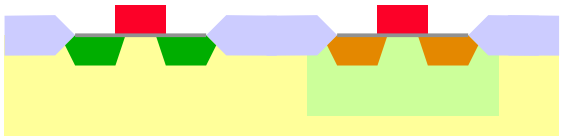
Making Transistors

3. Etch the poly





4. Implant source and drain



5. Coat the top of the poly and diffusion with metal to reduce resistance. (silicide)

Notice that the diffusion regions are formed in a self-aligned process. An oversized implant mask is used, but the field oxide and poly themselves actually define the diffusion regions. So, difficult alignment is avoided.

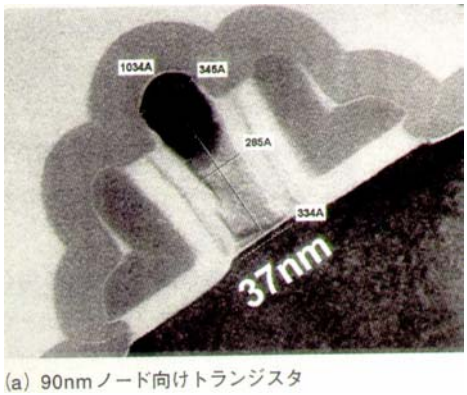
Actual Transistors

TSMC 0.13μ

Source: Nikkei Microdevices 11/00

TI 0.09μ

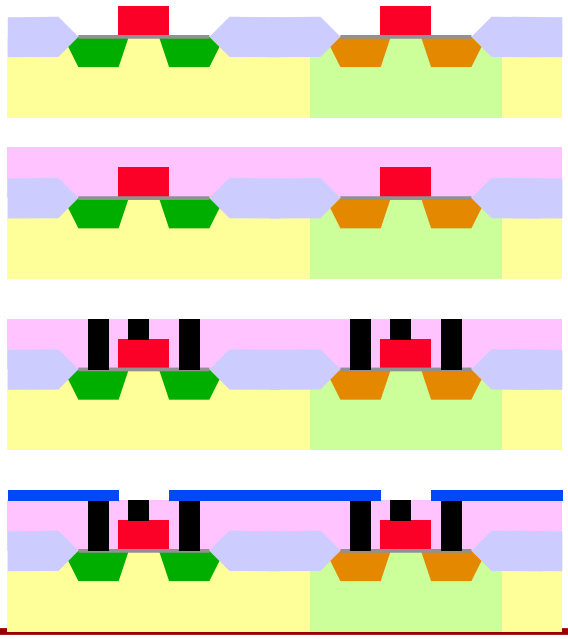
Source: Nikkei Microdevices 9/02



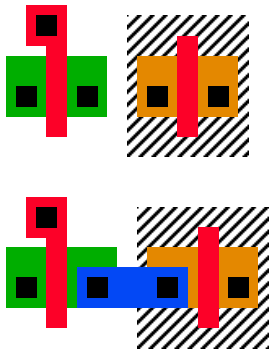
- Much more complex structure generated from drawn polysilicon gate

Making Wires

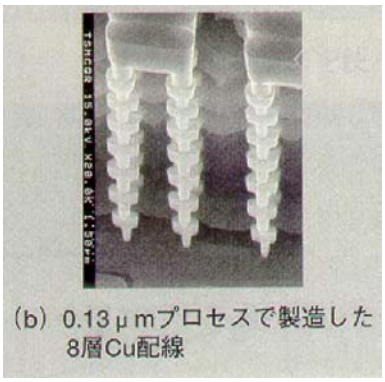
1. Deposit insulator may be polished to make it flat
2. Etch contacts to Si fill with conductor
3. Pattern metal wires



Can repeat these steps to make multiple levels of metal



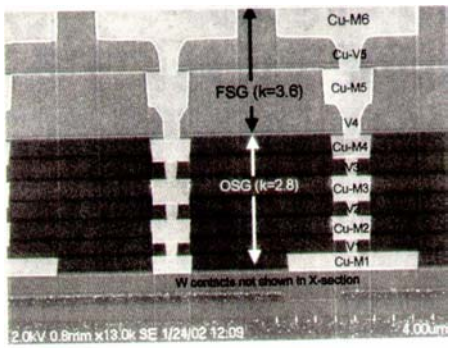
Actual Wires



TSMC
0.13μ
8 layers
Cu

Source: Nikkei Microdevices 11/00

TI
0.09μ
6 layers
Cu



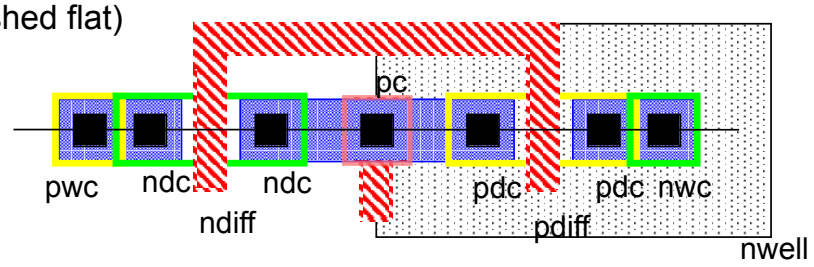
(b) 90nmノード向け多層配線

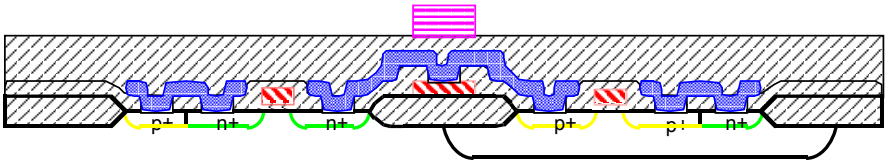
Source: Nikkei Microdevices 9/02

- 6-8layers of metal
- Vias and wires manufactured at same time (dual damascene)
- Top levels are thicker for power distribution
- Interlayer dielectrics are not all SIO_2 ($\varepsilon_r < 3.9$)

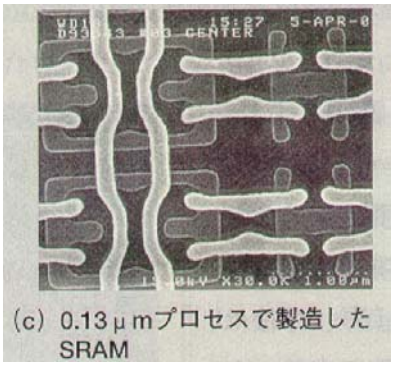
Layout View

- Layout of cell and final cross-section. This one has well contacts. In this cross section the M1 oxide was not planarized (polished flat)





Real Layout View



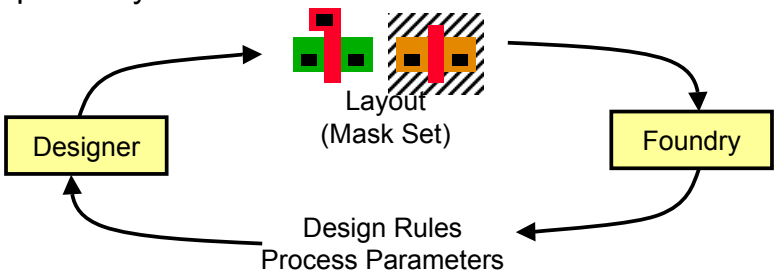
TSMC 0.13μ SRAM cell (Diffusion and poly)

Source: Nikkei Microdevices 11/00

- Note that things get rounded in manufacture

Fabrication Information

- Now that we know what fabrication is trying to do, how do we tell them precisely what to build?



- We don't care about the real details of the fab, but we have to define the patterning of the layers (that meet their rules) to specify our design.
- Sometimes knowing more about the fab details is useful when you need to debug a part.

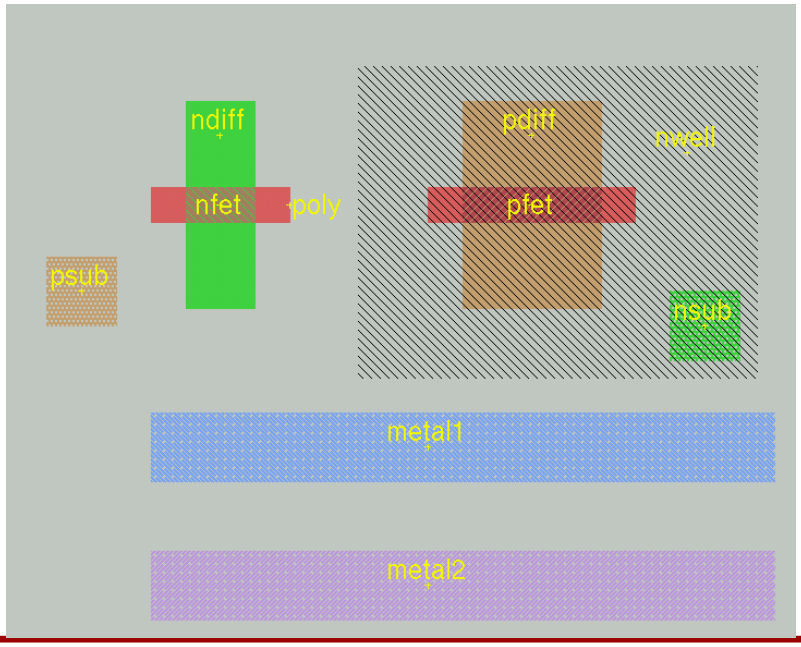
Layer Choice

- The layers a designer uses is generally set by the CAD tool.
- Our layout editor is 'Magic'
  - Magic is quick to learn and commonly available.
  - Primarily Paint (Color)-based, not object-based.
  - Highlighting of Electrically connected paint.
  - Interactive DRC checking.
- We will use the SCMOS design technology with Magic (MOSIS rules)

Magic SCMOS Layers

- We will use the Magic set of layers for the MOSIS technology SCMOS.
- There are 4 types of diffusion
  - Normal diffusion (forms transistors)
    - ndiff
    - pdiff
  - Diffusion for well contacts (same physically, but different function)
    - nohmic
    - pohmic
- Other layers are normal
  - Poly
  - Metal1
  - Metal2

Layer Example



Magic Contacts

ndc - ndiff to metal1

pdc - pdiff to metal1

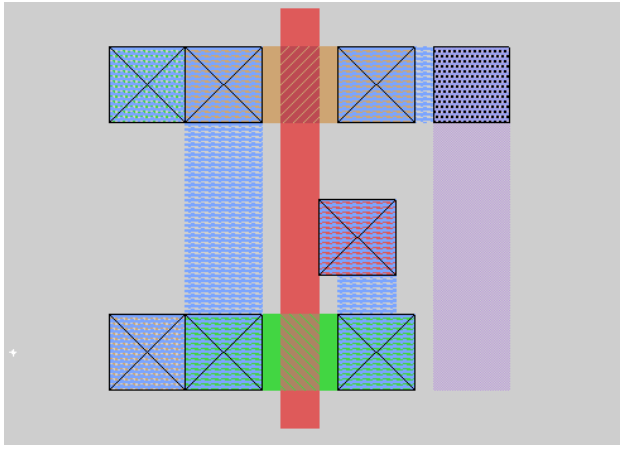
ppc - ppd to metal1

nnc - nnd to metal1

pc - poly to metal1

via - metal1 to metal2

Contact Example



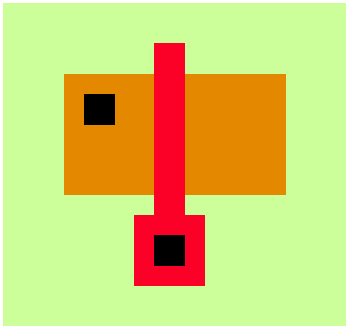
Fabrication Constraints on Layout

Fabrication places many constraints on the layout

- In EE271 we will worry about the two main types of constraints:
  - Resolution constraints
    - What is the smallest width feature than can be printed
    - What is the smallest spacing that will guarantee no shorts
    - Depends on lithography and processing steps that follow
    - Resolution often depends on the smoothness of the surface
      - (need to keep the image in focus, since depth of field is small)
      - Most modern processes are planarized, to keep surface flat
  - Alignment/overlap constraints
    - Like printing a color picture, need to align layers to each other
    - Need to choose which layer to align to
      - That layer will have better registration than the others.

Geometric Design Rules

- Resolution
  - width and spacing of lines on one layer
- Alignment
  - to make sure interacting layers overlap (or don't)
  - contact surround
  - poly overlap of diff
  - well surround of diff
  - contact spacing to unrelated geometry



Design Rules

- Most processes have design rules that are expressed in absolute physical units
  - poly width 0.3μm
  - poly spacing 0.3μm
  - metal width 0.5μm
  - metal spacing 0.5μm
- Typically not multiples of one another
- Using process-specific design rules gives the densest layout but is difficult to master
- We will express our design rules in lambda (λ) units
  - λ is half the drawn gate length (poly width)
  - All other design rules are expressed in whole multiples of λ
    - poly width 2 λ, space 3 λ
    - metal width, space 3 λ
  - usually requires rounding up
  - rules are scaled to generate masks for a variety of processes

SCMOS Lambda (λ) Design Rules

- We will be using the MOSIS SCMOS design rules
  - They are a simplified set of rules
  - Allow you to send your designs to a number of fab lines
  - Rules are based on λ, a type of scaling constant
  - λ was initially 1.5 μ, and now it is 0.15 μ in advanced fab lines
- Ignores some of the ways to save area (so extra conservative)
  - Use only Manhattan Layouts
  - Use only 90^{o} angles
- Companies regularly do design scaling, even if they don't use the symbol λ

SCMOS Design Rule Highlights

Resolution rules:

LAYER	WIDTH	SPACE
poly	2	3
diff	3	3
metal1	3	3
metal2	3	4
nwell	10	9
cut	2	2
via	2	3

Alignment rules:

cut/via surround	1
poly overlap diff	2
poly space to diff	1

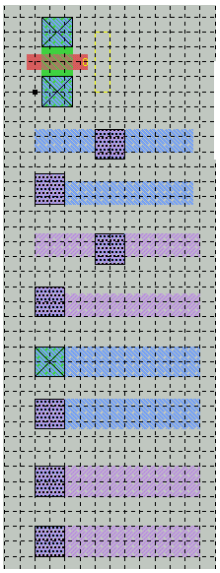
Notes:

Cut plus surround is 4
causes layout to fall on an 8λ grid

Pitch

Pitch is the repeat distance between objects

- 8λ = Contacted Transistor Pitch
  - Cut + PolyWidth + 2*Cut-to-Poly
- 6.5λ = Semi-Contacted Metal1 Pitch
  - (Contact + Width)/2 + Spacing
- 7.5λ = Semi-Contacted Metal2 Pitch
  - (Contact + Width)/2 + Spacing
- 7λ = Fully-Contacted Metal1 Pitch
  - Contact + Spacing
- 8λ = Fully-Contacted Metal2 Pitch
  - Contact + Spacing



+ Contact Rules

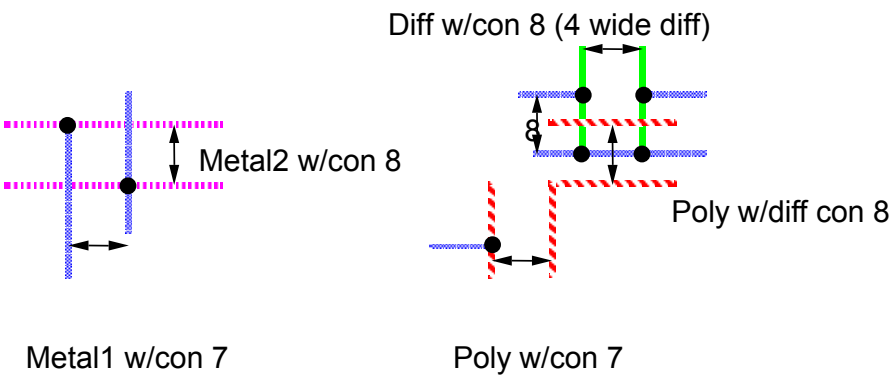
- In SCMOS, the spacing from contacts is often slightly larger than base material
  - Poly contact to poly spacing 3λ
  - Diffusion contact (ndc, pdc, nwc, pwc) to diffusion is 4λ
- This is done so the fabricator can make the surround of the actual contact cut slightly larger than 1λ if needed

The Magic Number "8"

- Most of the important rules for estimating the size of stick diagrams can be approximated by 8λ

Metal Pitch

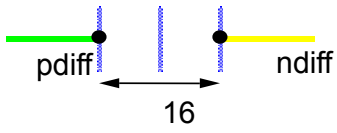
Diff / Poly Rules

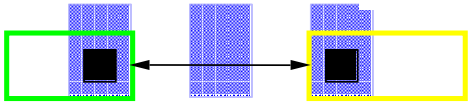


+ Hard Rules

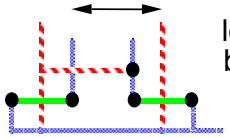
- There are two rules that don't fit into the nice "8" approach
- Well rules
  - The spacing between pdiff and ndiff is 10
  - While this is larger than 8, it is not a problem
  - Route at least one wire between gap

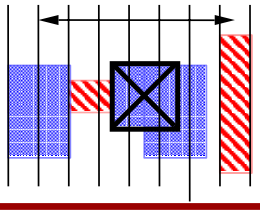
You don't need to worry about these rules at first. After doing some layout, you might check back to see if these rules explain some of the problems you have been experiencing.





- Poly Contacts





Using the Design Rules

While the Magic SCMOS design rules are simplified, there are still a number of rules to remember. A good way to start is to begin with a stick diagram of the cell you want to layout. Then you can use a subset of the rules to estimate what the layout will look like, and if it meets your standards you can begin the actual layout. While Magic makes layout easier, it always a good idea to have a plan on where things go before you start.

- **Warning**:

  While layout is often (sometimes) fun to do, it easily can be become an infinite time sink – one can always find a way to shrink the cell a few more microns. You should really have a plan BEFORE you start layout, and have a set constraints you are trying to achieve so you know when you are done.

Stick Diagrams

A stick diagram is like a layout:

- Contains the basic topology of the circuit
- The relative positions of the objects are roughly correct
  - Transistor 1 is to the right of transistor 2, and under transistor 3
- Each wire is assigned a layer, and crossing wires must be on different layers

But

- Wires are drawn as stick figures with no width
- The size of the objects is not to scale
- If you forgot a wire you can squeeze it in between two other wires
- It does not have to be beautiful

No matter how good the CAD tools is, it is still faster to draw a stick diagram first with pencils and paper (not beautiful is a big win).

- Layout Issues

In CMOS there are two types of diffusion

- ndiff (green)
  - Poly crossing ndiff makes nMOS transistors
- pdiff (yellow / brown)
  - Poly crossing pdiff makes pMOS transistors

Be careful, ndiff and pdiff are different

- You can't directly connect ndiff to pdiff
  - Must connect ndiff to metal and then metal to pdiff
- Can't get ndiff too close to pdiff because of wells
  - Large spacing rule between ndiff and pdiff
  - Means you need to group nMOS devices together and pMOS devices together

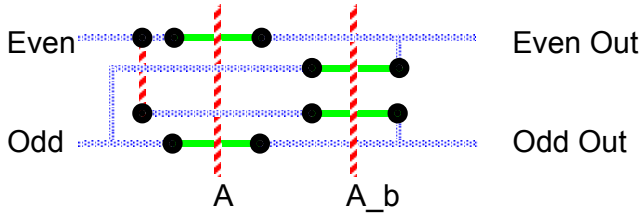
Basic Layout Planning

Here are a few simple guidelines to CMOS layouts

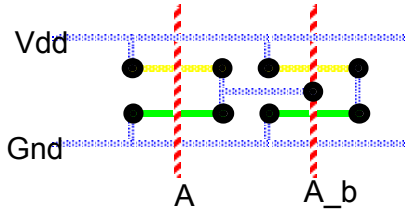
- You need to route power and ground. (in metal)
  - No one will auto connect it for you.
- Try to keep nMOS devices near nMOS devices and pMOS devices near pMOS devices.
  - So nMOS usually are placed near Gnd, and pMOS near Vdd
- Run poly vertically and diffusion horizontally, with metal1 horizontal (or the reverse, just keep them orthogonal)
  - Good default layout plan
- Keep diffusion wires as short as possible (just connect to transistor)
- All long wires (wire that go outside a cell, for example) should be in either m1 or m2.
- Try to design/layout as little stuff as possible (use repetition/tools)
  - Critical issue

- Typical Cell Layout Plan

- Look at the Parity from Lecture1
  (note: no pMOS and no Vdd Gnd) (very unusual)

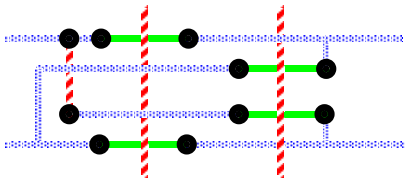


- CMOS Inverter uses same plan:



- Example of Size Estimation.

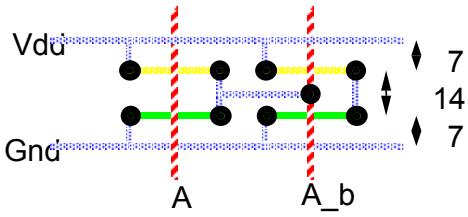
- Parity



8 * (3 tall +1 for space to next cell) = 32λ tall

8 * (4 wide +1 for space to next cell) = 40λ wide

- CMOS Inverter has similar size estimate:



While the actual spacing are a little different from the 8 rule, I would use the 8 rule for estimates. The numbers will be close.

- The distances shown are from a line at the center of the object (contact or wire) to the center of the next contact or wire. Remember that you are measuring from the center of each object...

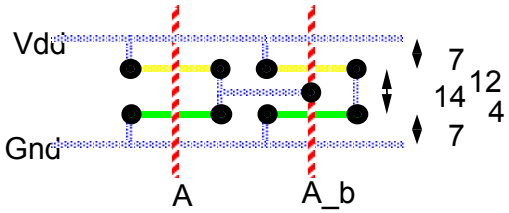
Estimating Layout Area from Sticks

- Draw your stick diagram
- Try to find the critical length path in X and in Y
- Count the number of contacted pitches
  - If transistors are not minimum width, remember to take that into account
- If you not happy with the answer, goto step 1 and try again.
  - Else you are done, and you can try to layout the cell.

- You will sometimes find out that you missed the real critical length path, but that is not unusual for people starting layout. You will get better at seeing the critical path as you do more layout.

- Size Estimation

- If the pMOS devices are 16λ wide and nMOS at 8λ wide



- Need to add (transistor width - 4) to previous estimates, so if we were going to use the rule of 8, we would get 8 + 16 + 8 like before, plus 12 (16 - 4) plus 4 (8 - 4), or 48.