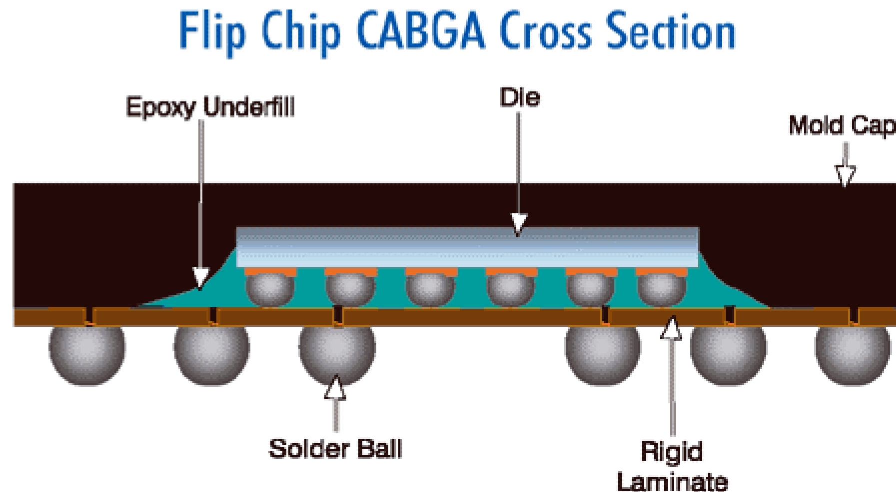
Additional Slides for Lecture 17

Advantages/Disadvantages of Wire Bonding

- Pros
  - Cost: cheapest packages use wire bonding
  - Allows ready access to front side of die for probing
- Cons
  - Relatively high inductance connections
    - Bond wires are 1nH/mm
    - Bond wire length is typically 3-5mm
  - Number of bonds is proportional to square root of die area
    - Not great for distributing large amounts of power
    - Not great for large numbers of I/O's

Connecting to the Die: Flip Chip

- Entire surface of die can be covered with bonding sites
  - Placed on 250μ centers
- Small balls (bumps) added at wafer level
- Chip flipped over and connected to package



Advantages and Disadvantages of Flip Chip

- Pros
  - Large number of connections
    - 1cm x 1cm wire bond chip @ 50μ staggered pitch: 800 pads
    - 1cm x 1cm flip chip @ 250μ centers: 1600 pads
  - Better power distribution
    - Flip chip: current flows through 20μ thick power plane routing
    - Wire bond: Current flows through 1μ thick top layer metal
- Cons
  - Cost
  - Debug

Integrated Circuit Packages

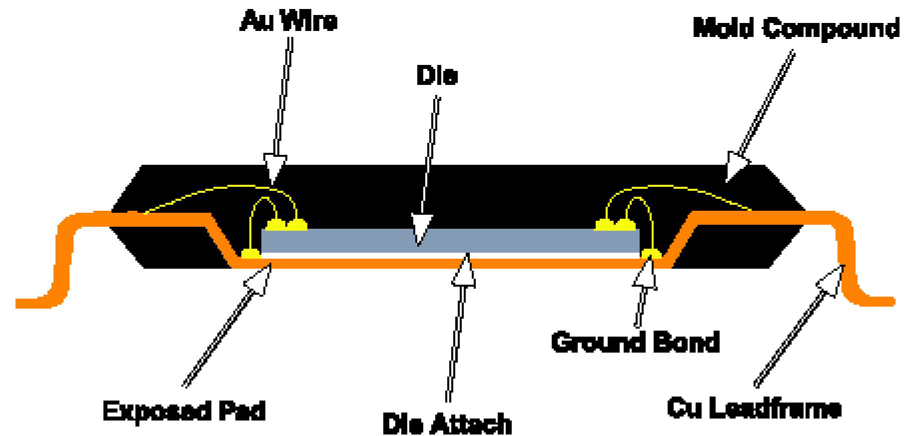
- Different applications have different requirements
  - Logic (Microprocessors, ASIC's)
    - high power, I/O count
    - Small number per board (ok if bigger)
    - Relatively high Average Selling Price (ASP)
  - Memory (DRAM, Flash)
    - Lower power and fewer I/O's per die
    - Large number per board (space at a premium
    - Cost cost cost…
- Package types vary by application

A Sampling of Packages

- Packages for Logic
  - QFP – Quad Flat Pack
  - BGA – Ball Grid Array
- Packages for Memory
  - TSOP – Thin Small Outline Package
  - CSP – Chip Scale Package

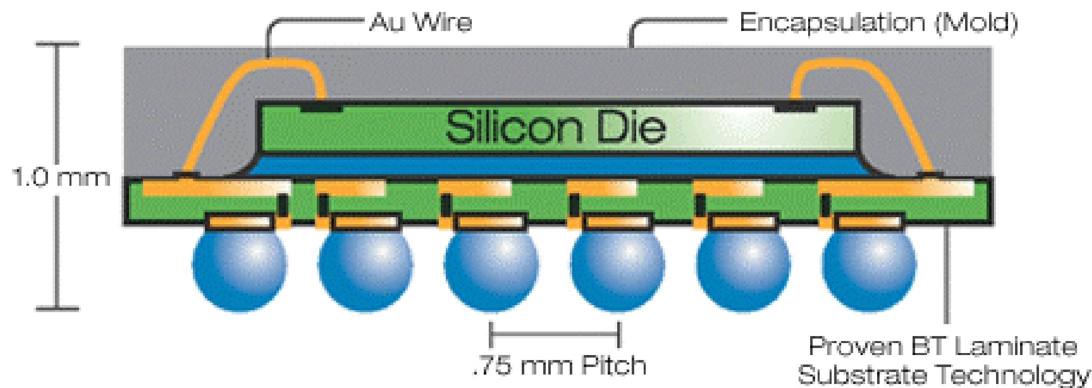
Quad Flat Pack (QFP)

- Wire Bond package
- Leads are coplanar fanning into die
  - Higher coupling



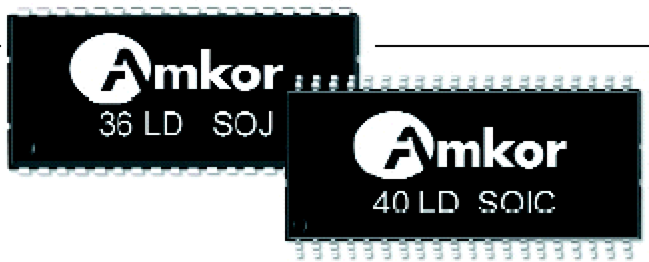
Ball Grid Array

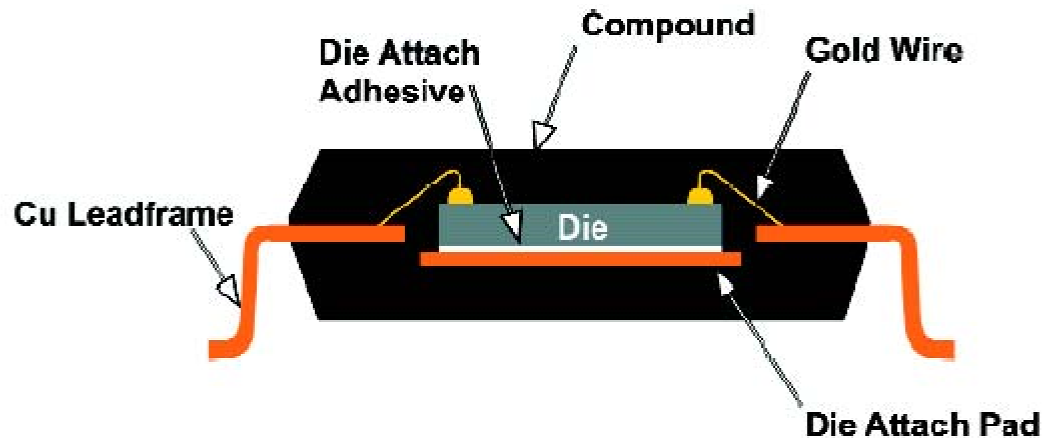
- Most popular ASIC package
  - Basically a small printed circuit board
- Multiple planes available in package
  - Possible to route larger numbers of signals
  - better signal integrity



Thin Small Outline Package (TSOP)

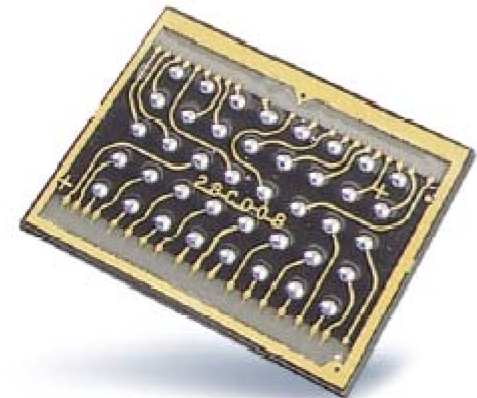
- Most popular DRAM package
  - Very cheap
- Wires bond to lead frame
  - Bond pads sometimes at center of die





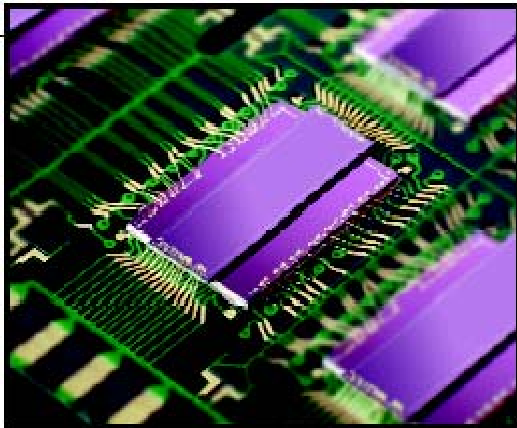
Chip Scale Packages

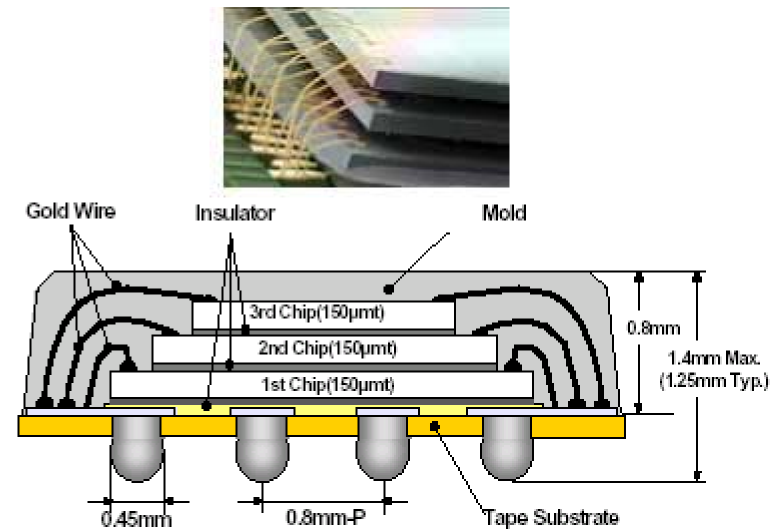
- Packages is same size as die
  - Very space efficient
- Very short leads – good electrical properties
- Back side of die exposed – good thermal properties
- Possible to fabricate at wafer level



Increasing Package Density

- Large memory systems, density is key
- For portable electronics, space is key
- Reduce required package size
  - Stack die on top of one another



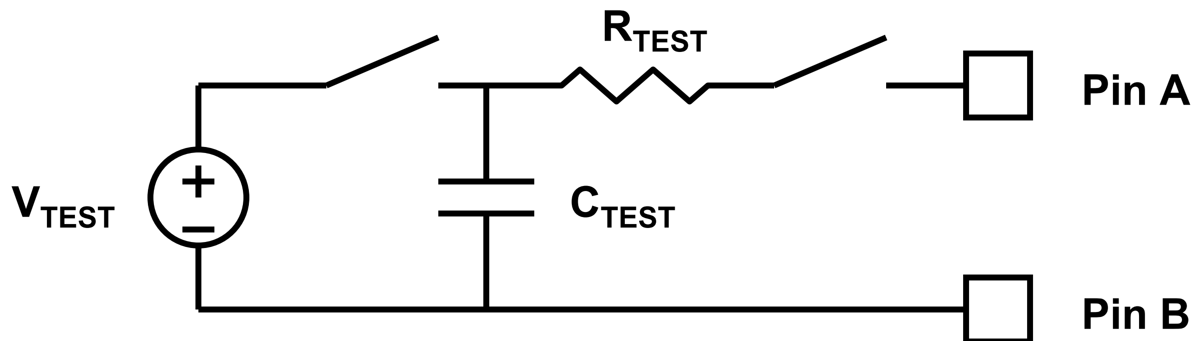


Electrostatic Discharge (ESD)

- MOS devices are very sensitive to high voltages
  - Gate oxides will fail if applied voltage is too high
  - Junctions will burn out if currents are too high
- These conditions can occur during ESD events
- All devices need to contain some type of ESD protection
- Challenges
  - Making sure the device survives the shock
  - Keeping the capacitance low enough to allow good I/O performance

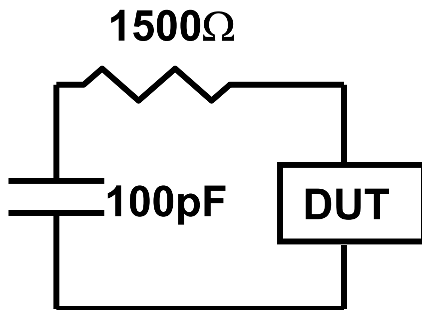
ESD Modeling and Testing

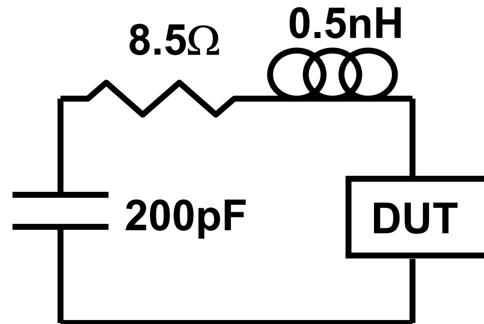
- Basic models exist for ESD
  - Charge up a capacitor to some test voltage V_{TEST}
  - Connect capacitor between two pins on device though R_{TEST}
- Apply between any pairs of signal pins
- Apply between all supplies and any signal pin

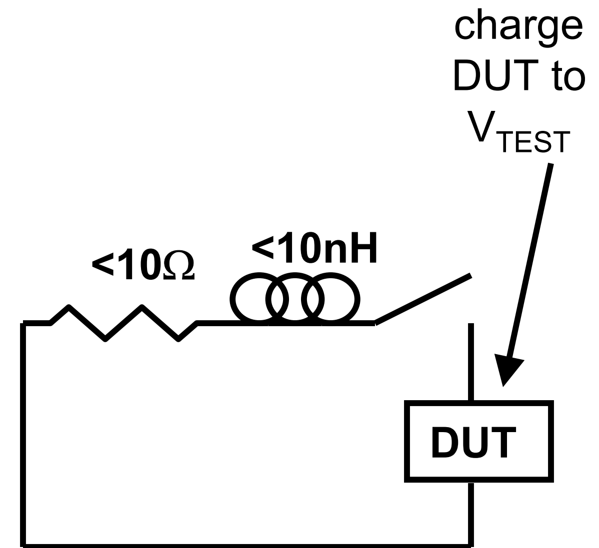


Different ESD Models

- Human Body Model (HBM)
- Machine Model (MM)
- Charged Device Model (CDM)





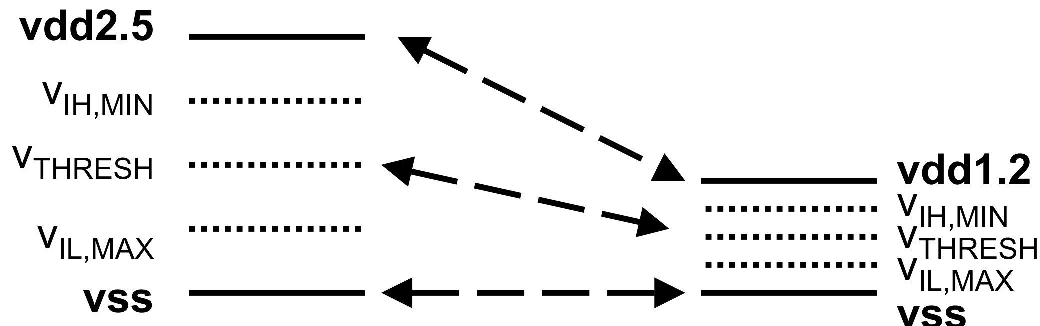


HBM	MM	CDM
V_{TEST} = 500V-4000V	V_{TEST} = 100V-400V	V_{TEST} = 200V-1000V
I_{Peak} = 350mA-2.5A	I_{Peak} = 1.5-6A	I_{Peak} = 2-10A

source: Dabral and Maloney: Basic ESD and I/O Design

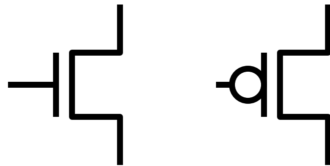
Providing for Voltage Compatibility

- Our new 0.13μ device with 1.2V supply needs to talk with older 2.5V or even 3.3V devices
- 1.2V output cannot reach the required level
- 1.2V input cannot survive the applied voltage
- How do we match these up?



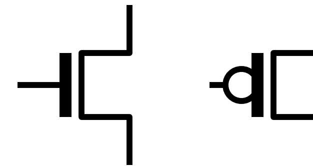
Process Support for I/O

- Newer processes have dual threshold devices
  - Fast, low voltage tolerance, thin oxide devices for core
  - Slow, higher voltage tolerance, thicker oxide devices for I/O
- Build most of chip from core devices
- Just build I/O drivers from thick oxide devices



Thin oxide devices

1.2V supply

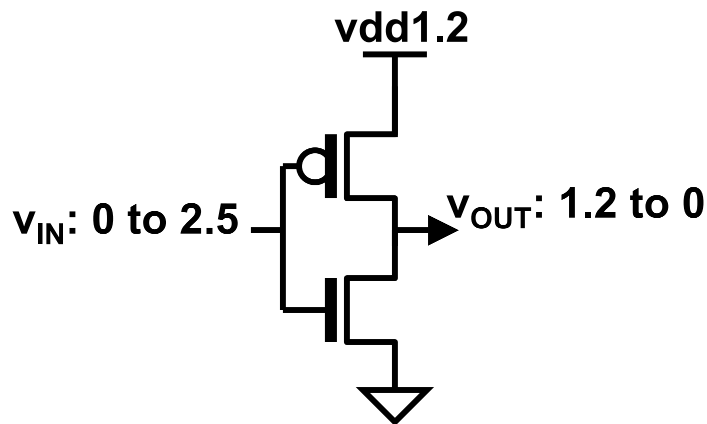


Thick oxide devices

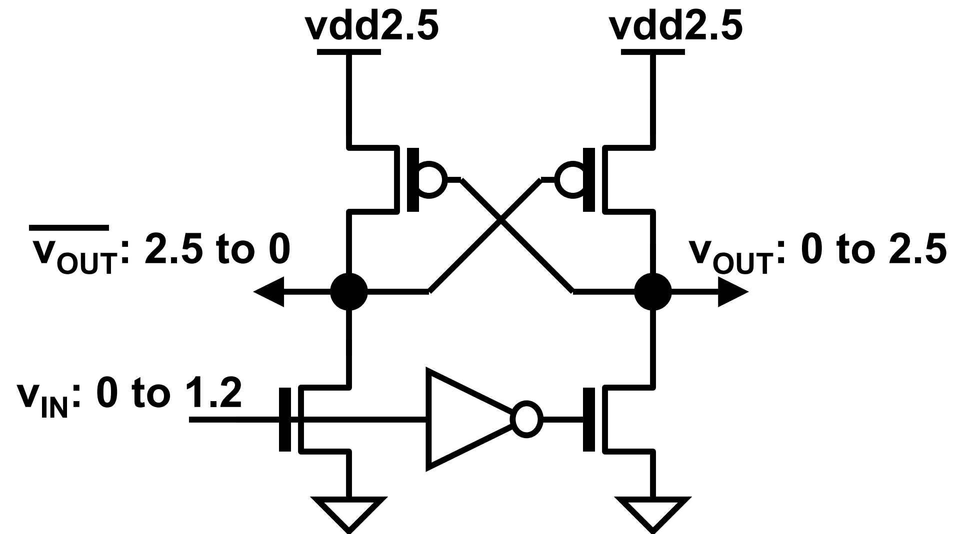
2.5V supply

Converting Levels

- How do we get from 1.2V domain to 2.5V domain?
  - 2.5V to 1.2V: Use thick oxide devices in inverter connected to low supply
  - 1.2V to 2.5V: Use level converter circuit



Input Buffer



Level Converter