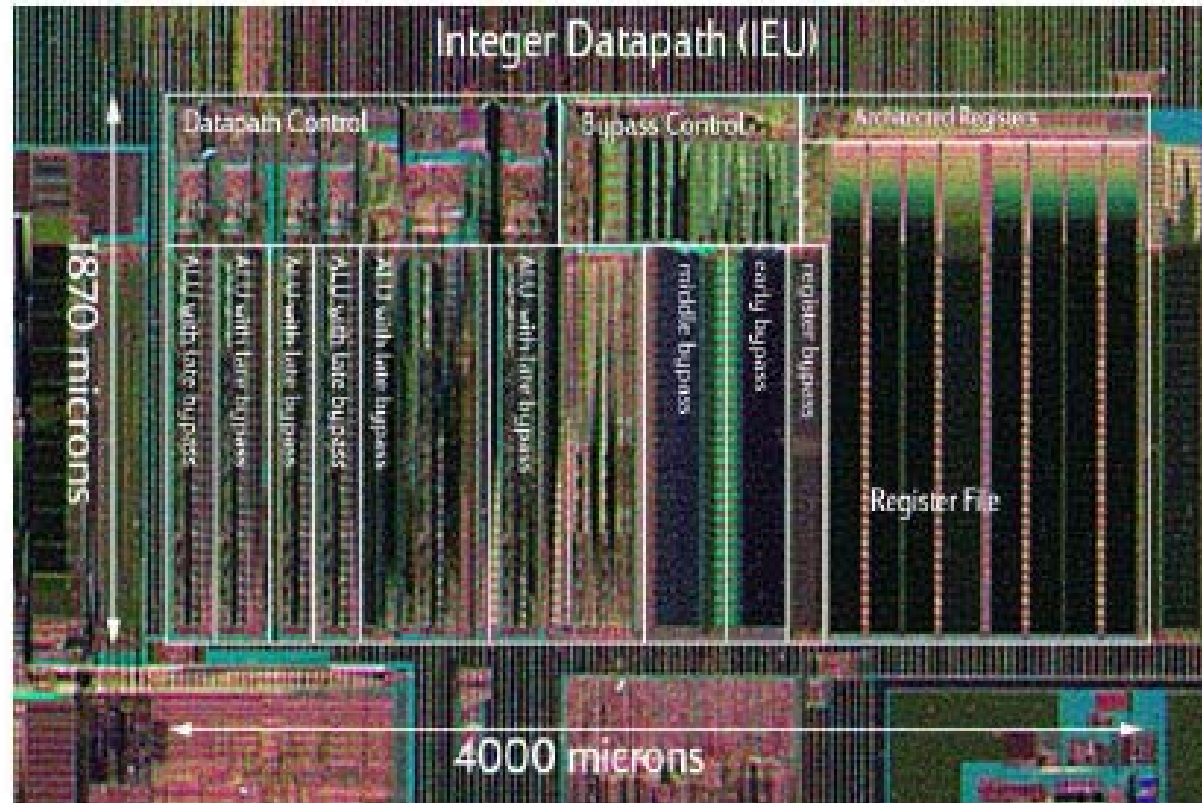


Itanium Integer Datapath

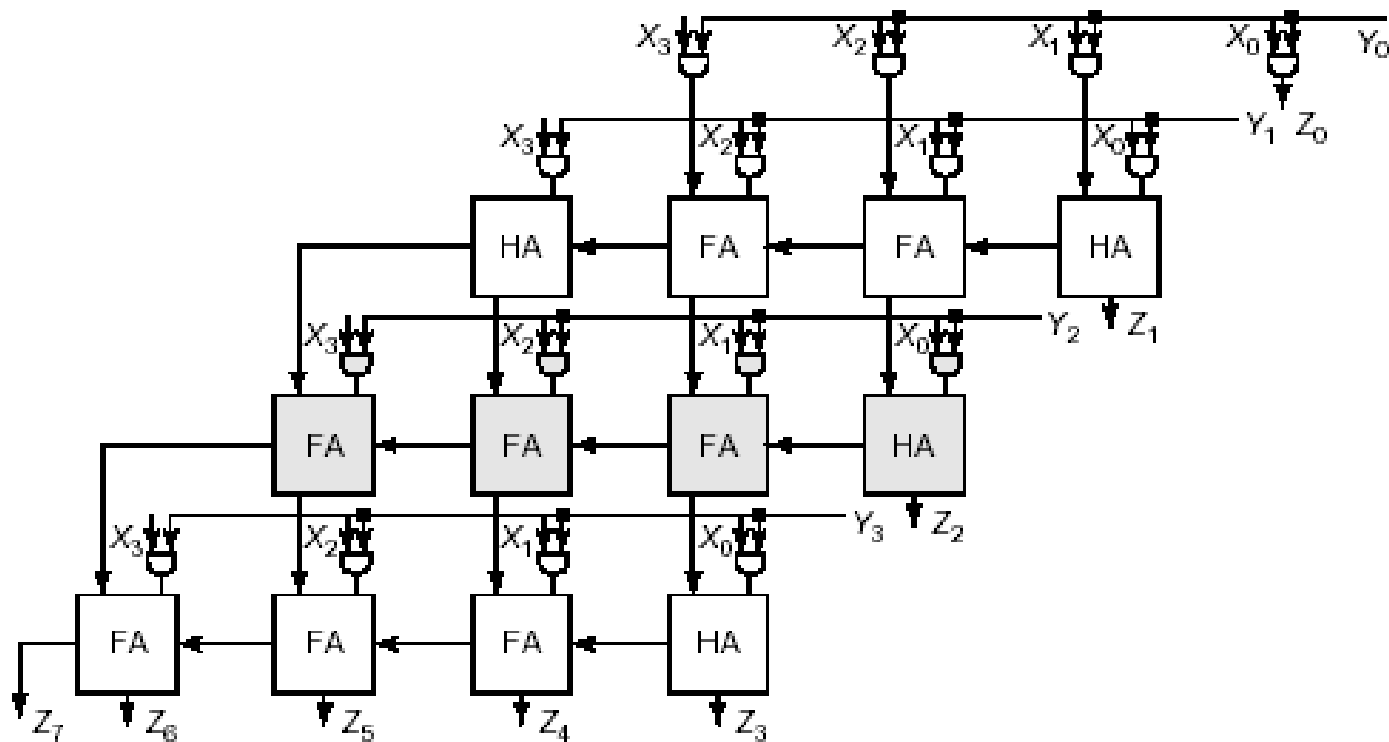
128 x 64 general registers

6 symmetrically bypassed 64 bit ALUs, 1 shifter

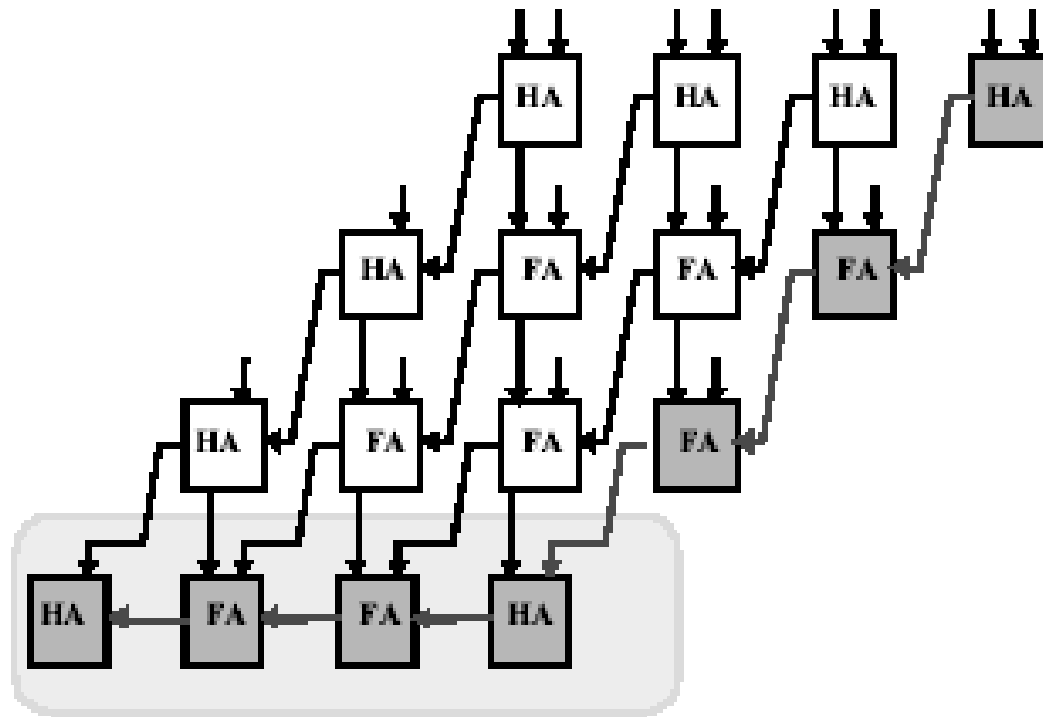


Fetzer, Orton, ISSCC'02

Array Multiplier



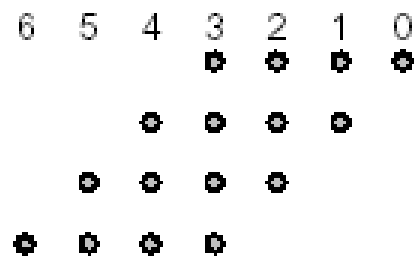
Carry-Save Multiplier



Vector Merging Adder

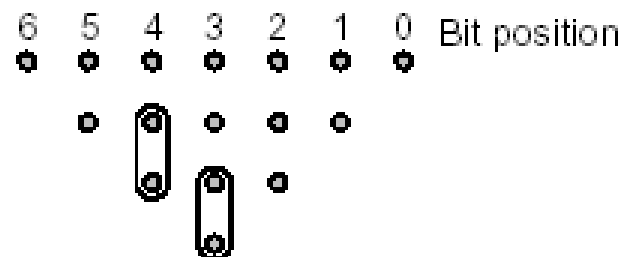
Wallace-Tree Multiplier

Partial products



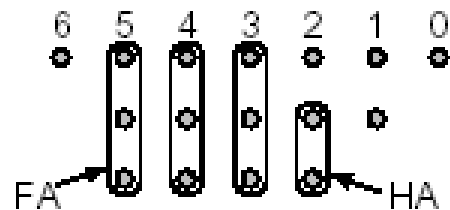
(a)

First stage



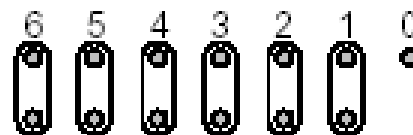
(b)

Second stage



(c)

Final adder



(d)